

Quad 2-input AND gate

74HC08; 74HCT08

FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to +85 °C and -40 to +125 °C.

DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC08	74HCT08	
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	C _L = 15 pF; V _{CC} = 5 V	7	11	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts;
 N = total load switching outputs;
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs.
2. For 74HC08: the condition is V_i = GND to V_{CC}.
 For 74HCT08: the condition is V_i = GND to V_{CC} - 1.5 V.

FUNCTION TABLE

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level;
L = LOW voltage level.

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ORDERING INFORMATION

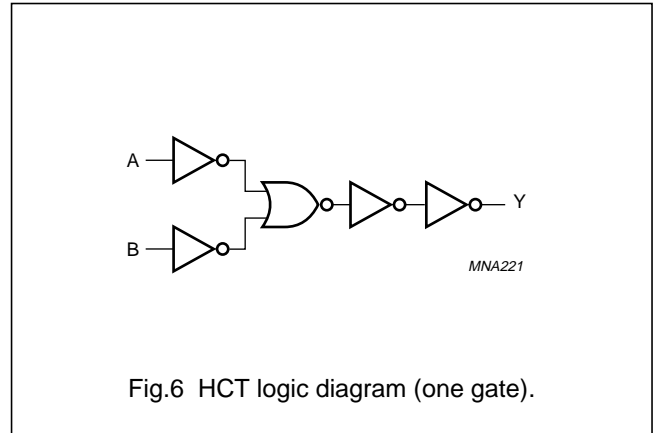
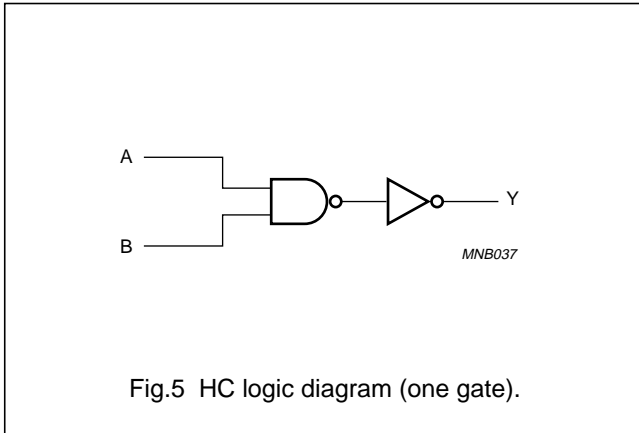
TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC08N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT08N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC08D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT08D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HC08DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT08DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC08PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT08PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC08BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT08BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V _{CC}	supply voltage

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC08			74HCT08			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	–	V _{CC}	0	–	V _{CC}	V
V _O	output voltage		0	–	V _{CC}	0	–	V _{CC}	V
T _{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t _r , t _f	input rise and fall times	V _{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V _{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V _{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		–0.5	+7.0	V
I _{IK}	input diode current	V _I < –0.5 V or V _I > V _{CC} + 0.5 V	–	±20	mA
I _{OK}	output diode current	V _O < –0.5 V or V _O > V _{CC} + 0.5 V	–	±20	mA
I _O	output source or sink current	–0.5 V < V _O < V _{CC} + 0.5 V	–	±25	mA
I _{CC} , I _{GND}	V _{CC} or GND current		–	±50	mA
T _{stg}	storage temperature		–65	+150	°C
P _{tot}	power dissipation				
	DIP14 package	T _{amb} = –40 to +125 °C; note 1	–	750	mW
	other packages	T _{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

- For DIP14 packages: above 70 °C derate linearly with 12 mW/K.
- For SO14 packages: above 70 °C derate linearly with 8 mW/K.
 For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

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Family 74HCT08

At recommended operating conditions; voltages are referenced to GND (ground = 0).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = 25 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –20 µA	4.5	4.4	4.5	–	V
		I _O = –4.0 mA	4.5	3.84	4.32	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±0.1	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±0.5	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	2	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	60	216	µA
T_{amb} = –40 to +85 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –20 µA	4.5	4.4	–	–	V
		I _O = –4.0 mA	4.5	3.84	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	20	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	270	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -20 µA	4.5	4.4	–	–	V
		I _O = -4.0 mA	4.5	3.7	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±10	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	40	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} - 2.1 V; I _O = 0	4.5 to 5.5	–	–	294	µA

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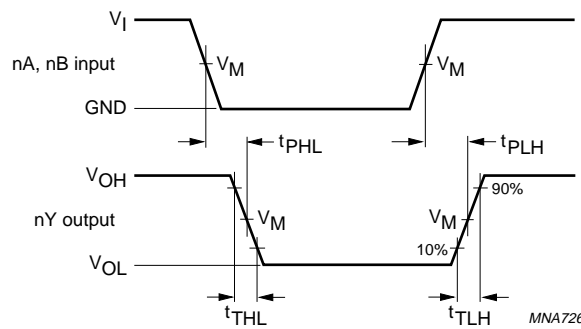
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Family 74HCT08

GND = 0 V; $t_f = t_r = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
$T_{amb} = 25$ °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	4.5	–	14	24	ns
t_{THL}/t_{TLH}	output transition time	see Figs 7 and 8	4.5	–	7	15	ns
$T_{amb} = -40$ to $+85$ °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	4.5	–	–	30	ns
t_{THL}/t_{TLH}	output transition time	see Figs 7 and 8	4.5	–	–	19	ns
$T_{amb} = -40$ to $+125$ °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	4.5	–	–	36	ns
t_{THL}/t_{TLH}	output transition time	see Figs 7 and 8	4.5	–	–	22	ns

AC WAVEFORMS



74HC08: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 74HCT08: $V_M = 1.3$ V; $V_I = \text{GND to } 3$ V.

Fig.7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

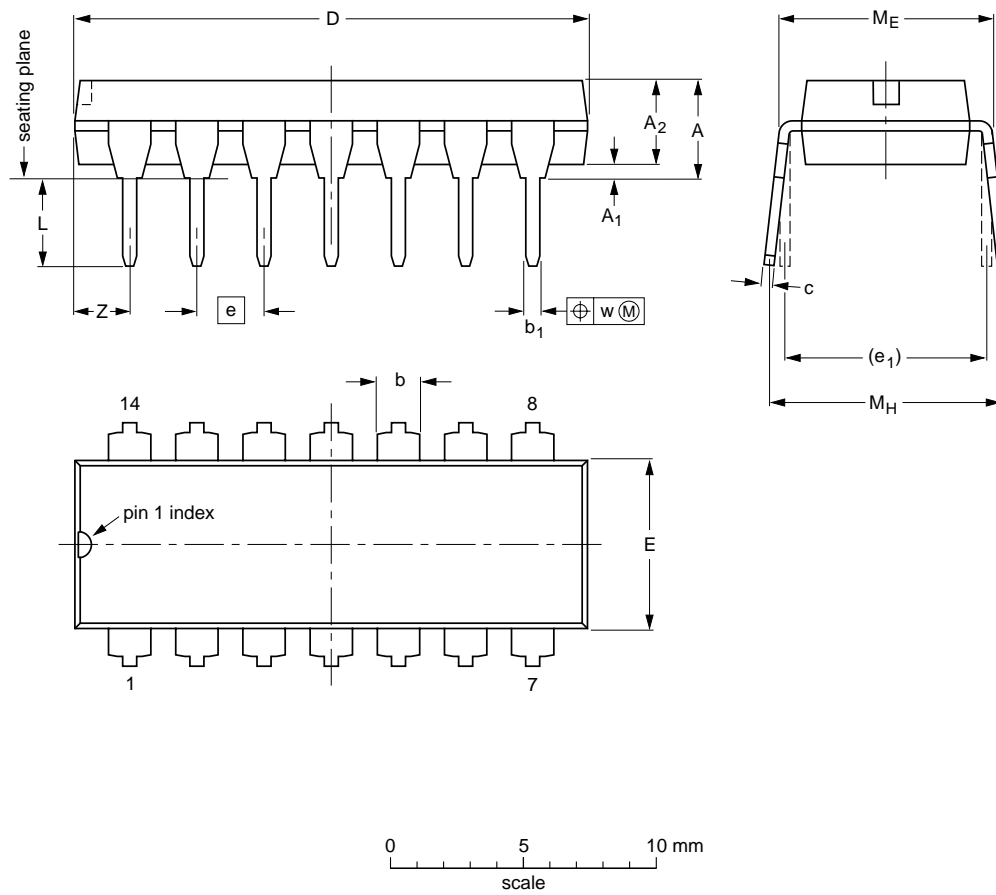
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PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

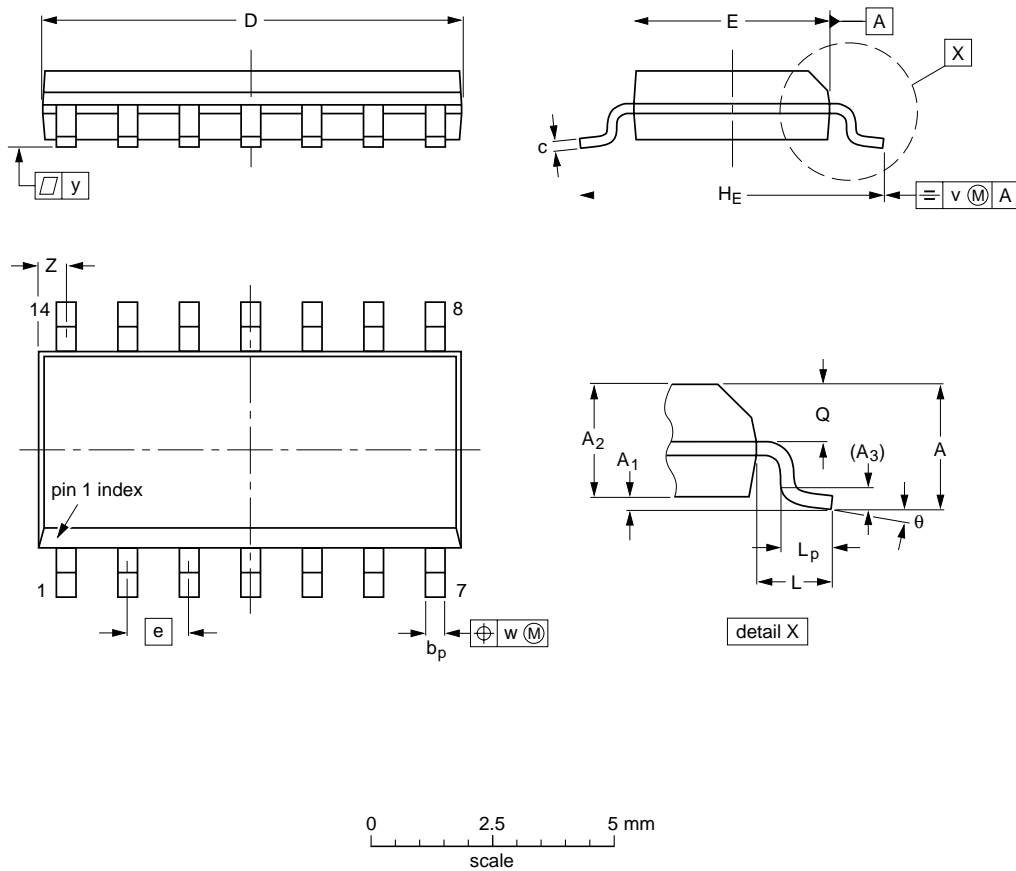
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT27-1	050G04	MO-001	SC-501-14	

Dual D-type flip-flop with set and reset;
positive-edge trigger

74HC74; 74HCT74

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT108-1	076E06	MS-012		